Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A scramble control method for a switching system, said switching system comprising:

a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports;

a plurality of input interfaces each connected to a corresponding input port of the switch, each of the input interfaces including a scrambler, each scrambler having a pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to the corresponding input port of the switch; and

a plurality of output interfaces each connected to a corresponding output port of the switch, each of the output interfaces including a descrambler, each descrambler having a pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from the corresponding output port of the switch to output frames of original data, and wherein each of the pseudorandom pattern generators of the scramblers and the descramblers generates a same pseudorandom pattern when initialized with a same input value,

said scramble control method comprising the steps of:

resetting the scramblers simultaneously to initialize the pseudorandom pattern generators of the scramblers with the same input value, so as to synchronize the scramblers;

resetting the descramblers simultaneously to initialize the pseudorandom pattern generators of the descramblers with the same input value, so as to synchronize the descramblers and to establish synchronization between the scramblers and the descramblers; and

continuously maintaining synchronization between the scramblers and the descramblers ~~after~~ when the switch performs a switching operation.

2. (Original) The scramble control method according to claim 1, wherein the scramblers and the descramblers operate according to a predetermined system clock, wherein

the scramblers are simultaneously initialized at a first time point and thereafter are not reset, and

the descramblers are simultaneously initialized at a second time point and thereafter are not reset, wherein the second time point is delayed from the first time point by a time period required for transferring a frame from an input interface to an appropriate output interface through the switch.

3. (Original) The scramble control method according to claim 2, wherein the first time point is a time when the switching system starts up.

4. (Original) The scramble control method according to claim 1, wherein the scramblers and descramblers are of frame synchronizing type.

5. (Previously Presented) The scramble control method according to claim 4, wherein a cycle of the pseudorandom patterns generated by the pseudorandom pattern generators of the scramblers and the descramblers is set to be longer than a length of the frame.

6. (Previously Presented) The scramble control method according to claim 5, wherein the pseudorandom pattern generators of the scramblers and the descramblers use a generator polynomial specified by: $1 + X^{43}$.

7. (Previously Presented) The scramble control method according to claim 1, further comprising the steps of:

determining, by a scrambler state generator, a scrambler state indicating a value of a pseudorandom pattern generated by the scrambler state generator, at predetermined intervals;

sending the scrambler state to the scramblers so that the scramblers are simultaneously reset to the value of the pseudorandom pattern indicated by the scrambler state; and

sending the scrambler state to the descramblers with a delay of a time period required for transferring a frame from an input interface to an appropriate output interface through the

switch, so that the descramblers are simultaneously reset to the value of the pseudorandom pattern indicated by the scrambler state.

8. (Original) The scramble control method according to claim 7, wherein the scramblers and descramblers are of frame synchronizing type.

9. (Previously Presented) The scramble control method according to claim 8, wherein a cycle of the pseudorandom pattern generated by the scrambler state generator is set to be longer than a length of the frame.

10. (Previously Presented) The scramble control method according to claim 9, wherein the scrambler state generator uses a generator polynomial specified by: $1 + X^{43}$.

11. (Previously Presented) A scramble control method for a switching system, said switching system comprising:

a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports;

a plurality of input interfaces each connected to a corresponding input port of the switch, each of the input interfaces including a scrambler, each scrambler having a pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to the corresponding input port of the switch; and

a plurality of output interfaces each connected to a corresponding output port of the switch, each of the output interfaces including a descrambler, each descrambler having a pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from the corresponding output port of the switch to output frames of original data, and wherein each of the pseudorandom pattern generators of the scramblers and the descramblers generates a same pseudorandom pattern when initialized with a same input value,

said scramble control method comprising the steps of:

at each of the scramblers,

generating a scrambler state indicating a value of a pseudorandom pattern generated by the pseudorandom pattern generator of the scrambler in frame timing;

assembling a frame including the scrambler state; and

transferring the frame including the scrambler state to the switch; and

at each of the descramblers,

receiving a frame including a scrambler state that is the scrambler state of a corresponding scrambler that assembled the frame; and

resetting the pseudorandom pattern generator of the descrambler to initialize the pseudorandom pattern generator of the descrambler with the value of the pseudorandom pattern indicated by the scrambler state, wherein the descrambler can be synchronized with the corresponding scrambler after the switch performs a switching operation.

12. (Original) The scramble control method according to claim 11, wherein the scramblers and descramblers are of self-synchronizing type.

13. (Original) The scramble control method according to claim 11, wherein the scramblers and descramblers are of frame synchronizing type.

14. (Previously Presented) The scramble control method according to claim 11, wherein a cycle of the pseudorandom patterns generated by the pseudorandom pattern generators of the scramblers and the descramblers is set to be longer than a length of the frame.

15. (Previously Presented) The scramble control method according to claim 14, wherein the pseudorandom pattern generators of the scramblers and the descramblers use a generator polynomial specified by: $1 + X^{43}$.

16. (Currently Amended) A switching system comprising:

a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports;

a plurality of input interfaces each connected to a corresponding input port of the switch, each of the input interfaces including a scrambler, each scrambler having a

pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to the corresponding input port of the switch;

a plurality of output interfaces each connected to a corresponding output port of the switch, each of the output interfaces including a descrambler, each descrambler having a pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from the corresponding output port of the switch to output frames of original data; and

a reset pulse generator for generating a scrambler reset pulse and a descrambler reset pulse, wherein the scrambler reset pulse is sent to all the scramblers at equal timing, and the descrambler reset pulse is sent to all the descramblers at equal timing;

wherein each of the pseudorandom pattern generators of the scramblers and the descramblers generates a same pseudorandom pattern when initialized with a same input value;

wherein the pseudorandom pattern generators of the scramblers are initialized to the same input value when the scramblers receive the scrambler reset pulse, so as to synchronize the scramblers;

wherein the pseudorandom pattern generators of the descramblers are initialized to the same input value when the descramblers receive the descrambler reset pulse, so as to synchronize the descramblers and to establish synchronization between the scramblers and the descramblers; and

wherein synchronization between the scramblers and the descramblers is continuously maintained ~~after~~ when the switch performs a switching operation.

17. (Original) The switching system according to claim 16, wherein the scramblers and the descramblers operate according to a predetermined system clock, wherein

the scramblers are initialized in response to the scrambler reset pulse and thereafter are not reset, and

the descramblers are initialized in response to the descrambler reset pulse and thereafter are not reset, wherein the descrambler reset pulse is delayed from the scrambler

reset pulse by a time period required for transferring a frame from an input interface to an appropriate output interface through the switch.

18. (Currently Amended) A switching system comprising:

a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports;

a plurality of input interfaces each connected to a corresponding input port of the switch, each of the input interfaces including a scrambler, each scrambler having a pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to the corresponding input port of the switch;

a plurality of output interfaces each connected to a corresponding output port of the switch, each of the output interfaces including a descrambler, each descrambler having a pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from the corresponding output port of the switch to output frames of original data; and

a scramble state generator for determining a scrambler state indicating a value of a pseudorandom pattern generated by the scramble state generator, at predetermined intervals;

wherein each of the pseudorandom pattern generators of the scramblers and the descramblers generates a same pseudorandom pattern when initialized with a same input value;

wherein the scrambler state is sent to the scramblers, and the scramblers are simultaneously reset to the value of the pseudorandom pattern indicated by the scrambler state, so as to synchronize the scramblers;

wherein the scrambler state is sent to the descramblers with a delay of a time period required for transferring a frame from an input interface to an appropriate output interface through the switch, and the descramblers are simultaneously reset to the value of the pseudorandom pattern indicated by the scrambler state, so as to synchronize the descramblers and to establish synchronization between the scramblers and the descramblers; and

wherein synchronization between the scramblers and the descramblers is continuously maintained ~~after~~ when the switch performs a switching operation.

19. (Previously Presented) A switching system comprising:

a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports;

a plurality of input interfaces each connected to a corresponding input port of the switch, each of the input interfaces including a scrambler, each scrambler having a pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to the corresponding input port of the switch; and

a plurality of output interfaces each connected to a corresponding output port of the switch, each of the output interfaces including a descrambler, each descrambler having a pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from the corresponding output port of the switch to output frames of original data,

wherein each of the scramblers further comprises:

a scramble state generator for determining a scrambler state indicating a value of a pseudorandom pattern generated by the pseudorandom pattern generator of the scrambler in frame timing; and

an assembler for assembling a frame including the scrambler state, and

each of the descramblers further comprises:

a reset circuit for resetting the pseudorandom pattern generator of the descrambler to a value of a pseudorandom pattern indicated by a received scrambler state included in a received frame that is received from the switch, said received scrambler state being the scrambler state of a corresponding scrambler that assembled the received frame;

wherein the descrambler can be synchronized with the corresponding scrambler after the switch performs a switching operation.

20. (New) The switching system of claim 19,

wherein the scramble state generator of each of the scramblers is configured to determine, for every frame to be output by the scrambler, a corresponding scrambler state

indicating a value of a corresponding pseudorandom pattern generated by the pseudorandom pattern generator of the scrambler in frame timing; and

wherein the assembler of each of the scramblers is configured to assemble, for every frame to be output by the scrambler, the frame including the corresponding scrambler state.

21. (New) The scramble control method of claim 11,

wherein the step of generating a scrambler state, comprises:

generating, for every frame to be output by the scrambler, a corresponding scrambler state indicating a value of a corresponding pseudorandom pattern generated by the pseudorandom pattern generator in frame timing;

wherein the step of assembling a frame, comprises:

assembling, for every frame to be output by the scrambler, the frame including the corresponding scrambler state; and

wherein the step of transferring, comprises:

transferring, for every frame to be output by the scrambler, the frame including the corresponding scrambler state to the switch.